UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/826,375	04/19/2004	Shahar Atir	P-6343-US	9730

56639 7590 05/15/2009

EMPK & Shiloh, LLP
c/o Landon IP, Inc.
1700 Diagonal Road
Suite 450
Alexandria, VA 22314

EXAMINER	
NGUYEN, VAN THU T	
ART UNIT	PAPER NUMBER
2824	

NOTIFICATION DATE	DELIVERY MODE
05/15/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PUSDKT@EM-LG.COM

Office Action Summary	Application No.	Applicant(s)	
	10/826,375	ATIR ET AL.	
	Examiner	Art Unit	
	VanThu Nguyen	2824	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 December 2008 and 18 January 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *12-17* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04/19/2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date ____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to Amendments filed on 12/23/2008 and 01/18/2009. Claims 1-11 are examined. Claims 12-17 have been withdrawn.

Claim Rejections - 35 USC § 112

2. Claims 5-6 and 10-11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding dependent claims 5, 6, 10 and 11, there is insufficient antecedent basis for limitation "wherein said coupling a sense amplifier ..." on lines 1-2 of each claims.

Regarding dependent claim 6 and 11, claim 1 lines 2-3 recites limitation "sensing substantially simultaneously a state of adjacent memory cells through at least a partially shared sensing path", which implies the source-side read operation is used (see specification of the present invention, paragraph [0032]). Claim 6, lines 2-3 recites "coupling said sense amplifier to bit lines of said adjacent cells that are not shared by said adjacent cells", which implies the drain-side read operation is used (see specification of the present invention, paragraph [0033]). There appears the source-side read operation and drain-side read operation can not be co-existed in the same read operation of the memory cells. Same rejection applied for claim 11.

There appears limitation "coupling a sense amplifier to a first source/drain terminal of each cell of said adjacent memory cells" claim 2 lines 2-3, is interpreted as more than one sense amplifier, e.g. two sense amplifiers. If so, there appears a conflict with limitation "coupling *said sense amplifier* to bit lines of said adjacent cells that are not shared by said adjacent cells" in

claim 6, lines 2-3 [emphasis added]. Besides, specification does not disclose both bit lines of the adjacent cells are coupled to the same sense amplifier. For the purpose of examination, Examiner interprets limitation in claim 6, lines 2-3 as "coupling *said* sense amplifiers to bit lines of said adjacent cells that are not shared by said adjacent cells".

Same rejection and interpretation applied for claim 11.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-8, 10-11 are rejected under 35 U.S.C. 102(b) as being anticipated by US 5,831,892 to Thewes et al. ("Thewes") or US 4,992,980 Park et al. ("Park").

Thewes reference:

Regarding independent claim 1, Thewes discloses, in FIG. 1, a method of reading data in a virtual ground array of memory cells comprising:

- sensing substantially simultaneously a state of adjacent memory cells, wherein a bit stored in each cell of said adjacent memory cells through at least a partially shared sensing path (see col. 1 ll. 6-12), wherein sensing includes applying a first voltage to a common word line (FIG. 1: switch $S'_{k,vwl}$ of the cells to be read out are closed, coupled the selected word line to V_{wl} of 5V, see col. 4 ll. 6-13) and a substantially similar voltage ~~to either a shared bit line or~~ to non-shared bit lines

(FIG. 1: connecting all non-shared bit lines BL_{n-3}, BL_{n-1} to the left of selected memory cells $Z_{n,k}$ and $Z_{n+1,k}$ to V_{gnd})

Regarding dependent claim 2, Thewes further discloses wherein said sensing substantially simultaneously comprises:

- coupling a sensing circuit to a first source/drain terminal of each cell of said adjacent memory cells (FIG. 1: coupling evaluation circuit AWS to bit line BLn);
- setting a voltage at a second drain/source terminal of each cell of said adjacent cells to a read level (FIG. 4: setting bit line BLn-1 to ground and bit line BLn to Vvm); and
- sensing in a reading direction the state of said adjacent cells (see col. 4 ll. 19-55).

Regarding dependent claims 3-5 and 10, Thewes further discloses wherein adjacent cells share a word line WL_k, an inside bit line BL_n, the evaluation circuit AWS coupled to the inside/shared bit line BLn,

Regarding dependent claim 7, Thewes inherently discloses wherein any one of said memory cells stores at least one bit in said charge trapping region (because the memory cells in Thewes are EPROM cells, see col. 3 ll. 6-15).

Regarding dependent claim 8, Thewes discloses wherein said adjacent cells are sense with substantially identical current (because they both have the same sense current).

Park reference:

Regarding independent claim 1, Park discloses a method of reading data in a virtual ground array of memory cells (see abstract) comprising:

- sensing substantially simultaneously a state of adjacent memory cells, wherein a bit stored in each cell of said adjacent memory cells through at least a partially shared sensing path (FIG. 3: simultaneously access memory cells 70a and 70b, and partially shared sensing path 76a), wherein sensing includes applying a first voltage to a common word line (i.e. selecting row line 61a, see col. 5 ll. 35-37) and a substantially similar voltage ~~to either a shared bit line or~~ to non-shared bit lines (i.e. maintaining lines 51-52 at precharge potential, see col. 5 ll. 64-66)

Regarding dependent claims 2, 6 and 10-11, Park further discloses wherein said sensing substantially simultaneously comprises:

- coupling a sense amplifier to a first source/drain terminal of each cell of said adjacent memory cells (e.g. coupling both memory cells 70a and 70b to their corresponding read path circuitry via lines 51 and 52, which are not shared by said adjacent memory cells, see col. 5 ll. 50-56 and FIG. 4);
- setting a voltage at a second drain/source terminal of each cell of said adjacent cells to a read level (e.g. discharge lines 70a to ground, see col. 5 ll. 45-49 and FIG. 4); and
- sensing in a reading direction the state of said adjacent cells (e.g. sensing currents in both memory cells 70a and 70b).

Regarding dependent claims 3-4, see FIG. 4 of Park.

Regarding dependent claim 7, Park inherently discloses wherein any one of said memory cells stores at least one bit in said charge trapping region (because the memory cells in Park are EPROM and subjected to programming and erasing).

Regarding dependent claim 8, it is clear that if adjacent memory cells store identical data, they will produce identical current when being accessed.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Thewes/Park in view of U.S. Patent No. 6,975,536 to Maayan et al. ("Maayan").

Thewes/Park discloses, as applied in prior rejection of claim 1, all claimed subject matter except further limitation as set forth in claim 9.

Regarding dependent claim 9, Maayan discloses, in FIG. 1, a virtual ground memory device comprising nitride read only memory (NROM) cells

Since Thewes/Park and Maayan are all from the same field of endeavor, the purpose disclosed by Maayan would have been recognized in the pertinent art of Thewes/Park.

It would have been obvious at the time the invention was made to a person having ordinary skill in the art to apply the method of reading disclosed in Thewes/Park for the NROM memory device in Maayan in order to shortening the duration of read time (see col. 1 ll. 6-11).

Response to Arguments

7. Applicant's arguments with respect to claims 1-11 have been considered but are moot in view of the new ground(s) of rejection.

35 U.S.C. 112 Rejections

Claim 6 fails to further limit the reading method of claim 1 because it recites a drain-side read operation (see specification, paragraph [0033]) while claim 1 recites a source-side read operation (see specification, paragraph [0032]). There appears the source-side read operation and drain-side read operation can not be coexisted in the same read operation of the memory cells.

35 U.S.C. 102 Rejections

Thewes reference:

Interpretation of non-shared bit lines are other bit lines except common bit line BL_n.

Park reference:

Applicant admits, in Remark filed on 12/23/2008, in a second case (i.e. drain-side read operation described in paragraph [0032] of the present invention), the non-shared bit line on the other side of each adjacent cell may be sensed while sensing current is provided through the shared bit line - the at least partially shared sensing path. Similar concept applied for Park, the shared bit line 76b between selected memory cells 70a and 70b is considered as the at least partially shared sensing path.

Conclusion

8. When responding to this office action, applicants are advised to provide the examiner with the line numbers and page numbers in the application and/or references cited to assist the examiner in locating appropriate paragraphs.

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VanThu Nguyen whose telephone number is (571) 272-1881. The examiner can normally be reached on Monday-Thursday, 9:00am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard Elms can be reached on (571) 272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

May 13, 2009

/VanThu Nguyen/
Primary Examiner
Art Unit 2824